Title of the Tutorial: Computational Lithography for advanced CMOS nodes

Abstract: Optical lithography is widely used for mass production of ultra large scale Integrated Circuits (ICs) because of its superiority in economic terms. The semiconductor industry has kept pace with the Moore’s law by steadily reducing the wavelength of light used in this optical lithography. In the past two decades, the wavelength used in optical lithography has shrunk down to today’s standard of 193nm. This strategy however has become less certain as wavelengths shorter than 193nm cannot be used without a major overhaul of the lithographic process. While new lithographic methods like EUV lithography are under development, the semiconductor industry is relying more on a relatively new field called “Computational Lithography”. Current optical lithography capabilities would have been impossible without the use of computational lithography tools and these techniques will only become very essential in the future. The Optical Proximity Correction (OPC) is one of the image enhancement techniques that nestle under the computational lithography umbrella. The success of these computational techniques relies heavily on the performance of lithography process models. Any small enhancement in the performance of process models can result in a valuable improvement in the yield. This tutorial is aimed to present an overview on the current challenges in optical lithography process faced by IC manufacturing industries and how computational lithography is helping the industry to address those challenges. The fundamental principles of resolution limit, lithography image formation, process model used for lithography simulation, resolution enhancement techniques, and next generation lithography techniques will also be discussed.

Duration: 3hrs

Prerequisite knowledge: The participants should be familiar with the IC manufacturing processing steps and should have some basic knowledge about photolithographic process.

Detailed outline: The Computational Lithography (CL) is very much essential for patterning nanometer long dimensions in advanced CMOS nodes. The CL comprises a broad set of techniques that use physics based calculations to eke out greater lithographic performance from a given generation of steppers. The accurate modeling of lithographic processes, sample preparation and selection for calibrating the models and computationally efficient execution are some requirements of CL. The successful R&D in CL has so far helped the semiconductor manufacturing industries in extending the life of optical lithography beyond previously forecast durations. This tutorial will cover the essentials of CL and will be done in two parts (90mins each).

Part 1: This part will mostly cover the introduction to optical lithography process. We will concentrate on the projection printing system, which uses an imaging lens. We will go through the illumination, the mask, the imaging lens and the photoresist. After that, we will discuss the motivation for CL. We will briefly discuss the device scaling and lithography trends. At the end of this section, we will discuss the resolution limit for lithography process defined by Rayleigh equation. This equation explains the minimum feature size, the size we’re interested in. We know that it is dependent on \( k_1 \) (lithography process parameter) multiplied by wavelength over NA (numerical aperture). The whole theory of lithography modeling and simulation revolves around these three parameters. These parameters will be explained in detail in this section.
Part 2: This part of the tutorial will start with the Resolution Enhancement Techniques (RETs). The RETs are methods used to modify photo-masks for integrated circuits (ICs) to compensate for limitations in the lithographic processes. We will discuss in details the various RET techniques such as, Optical Proximity Correction (OPC), Sub-Resolution Assist Features (SRAF), Phase Shift Mask (PSM), Off-Axis Illumination (OAI), Source Mask Optimization (SMO), Inverse Lithography (ILT), and Multi-Patterning Techniques. The OPC is a most important RET techniques and the basic operations of OPC technique will be explained using examples.

The tutorial will end with the summary of computational lithography current challenges and future solutions.

Tutorial goals:

- To understand the lithography process as a whole
- To understand the resolution limits and fundamental principles of image formation in lithography printing.
- To know about the key issues in lithography printing and resolution enhancement techniques
- To understand the OPC operations.
Background information of the presenter(s)

Presenter 1:
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Bio: NiharRanjanMohapatra is currently working as an Associate Professor at IIT Gandhinagar. Prior to joining IIT Gandhinagar as an Assistant Professor in July 2011, he worked in semiconductor industries like IHP Microelectronics, Advanced Micro Devices (AMD) and Globalfoundries for eight years. During that time he worked on CMOS technologies starting from 130nm till 28nm. In his last assignment at GLOBALFOUNDRIES, he was responsible for integrating several memory devices (SRAM, eDRAM and NVM) in 28nm bulk CMOS technologies. His current research interests are in nanoelectronic devices, CMOS technology, CMOS device and process development, compact modelling, semiconductor device reliability, computational lithography and analog circuit design. He has authored and co-authored several papers on international journals and conference. He has also received research funding from several public and private organizations including Department of Science and Technology, Ministry of Electronics and Information Technology, Indian Space Research Organization, GLOBALFOUNDRIES etc.
Presenter 2:
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Bio: Pardeep Kumar received his master’s degree in VLSI Design & CAD from Thapar University, Patiala, India in 2012. Currently, he is working as a MTS with computational lithography group at GLOBALFOUNDRIES Bengaluru. He is also working towards the Ph.D. degree in the area of computational lithography at the Indian Institute of Technology (IIT) Gandhinagar, Gandhinagar, India. His current research interests include the computational lithography, lithography process models and data analytics.