VDAT 2017 Program (Tentative)	
29th June 2017 (DAY 0) All the Tutorial will be held at the Management Block	
Time	**Event**
08:00 AM to 09:30 AM	Registration **(Department of Management Studies)**
09:30 AM to 11:00 AM	Tutorial 1 LH 1
	Tutorial 2 LH 2
	Tutorial 3 LH 3
11:00 AM to 11:15 AM	Tea Break
11:15 AM to 12:45 PM	Tutorial 1 LH 1
	Tutorial 2 LH 2
	Tutorial 3 LH 3
12:45 PM to 02:00 PM	Lunch Break
02:15 PM to 03:45 PM	Tutorial 4 LH 1
	Tutorial 5 LH 2
	Tutorial 6 LH 3
03:45 PM to 04:00 PM	Tea Break
04:00 PM to 05:30 PM	Tutorial 4 LH 1
	Tutorial 5 LH 2
	Tutorial 6 LH 3
07.30 PM	Dinner
Tutorial 1: Achieving the Best STA Accuracy for Advanced Nodes, Gauri Sankar Malla, Synopsys India Pvt. Ltd., India	
Tutorial 2: Computational Lithography for Adavanced CMOS Nodes, N.R.Mohapatra, IIT Gandhinagar and Mr. Pardeep Kumar, Global Foundaries, Bangalore	
Tutorial 3: Circuit and System Design Issues for IoT Sensor Node, M.Hasan, AMU	
Tutorial 4: Design of Modern mm-Wave Transmitters and Power Amplifiers in Silicon and FD SoI CMOS, K. Bhattacharya, Amrita University, Coimbatore	
Tutorial 5: Transaction Level Modelling with System C For System Level Design, Nishit Gupta, Microelectronics Development Division, Ministry of Communication and Information Technoogy, Govt. of India and Deepak Jharodia, ST Microelectronics	
Tutorial 6: Advanced Analog Design, HS Jatana and Ashutosh Yadav, SCL Chandigarh, India	

VDAT 2017 Program (Tentative)	
30th June 2017 (Day-1)	
Registration (MB Foyer + MAC)	
Time	**Event**
08:00 AM - 9:15 AM	Breakfast (Ravindra Bhawan Lounge)
09.00 AM - 9.45 AM	Opening Ceremony (MAC) (Chief Guest: Dr.V.K.Saraswat, Padma Shri, Padma Bhushan, Member NITI Aayog)
9.45 AM - 10:30 AM	Plenary – I (MAC) (Prof. Jagadesh Kumar, Vice-Chancellor, JNU)
10:30 AM - 11.00 AM	High Tea (Mac Lounge)
11.15 AM - 01.15 PM	D1-IA, 5 Papers (4 long + 1 short Presentation) Digital Design
	D1-IB, 5 Papers (4 long + 1 short Presentation) Analog/Mixed Signal
01:15 PM to 02:15 PM	Lunch Break (Ravindra Bhawan Lounge)
02:15 PM to 03:00 PM	**Invited Speaker – 1 (Prof. P.Chakrabarti, IIT-BHU)**
03:00 PM to 3:45 PM	**Invited Speaker – 2 (Dr Devesh, Dwivedi, Global Foundaries, Bangalore)**
3:45 PM to 4:20PM	Poster Presentation (2 minutes per poster)
04:20 PM to 4:45 PM	Coffee break
04:45 PM to 06:45 PM	D1-II A VLSI Testing
	D1-II B Devices and Technology-I
8:30 PM to 9:15 PM	Banquet Talk (MAC Auditorium)
09.15 PM	Banquet (Ravindra Bhawan Lounge)

Posters (2 Minutes Each) to be continued on DAY 2 also.
35, 45, 54, 58, 77, 102, 106, 114, 121, 128, 143, 163, 173, 193, 202, 231, 264, 268.

Digital Design	
PID 213: VLSI Implementation of Throughput Efficient Distributed Arithmetic Based LMS Adaptive Filter Mohd Tasleem Khan and Shaik Ahamed.	**PID 76: Flexible Composite Galois Field GF ((2^m)^ 2) Multiplier Designs** Mohamed Asan Basiri M and Sandeep K Shukla.
PID 100: Estimating the Maximum Propagation Delay of 4-bit Ripple Carry Adder using Reduced Input Transitions Manan Mewada, Mazad Zaveri and Anurag Lakhlani.	**PID 246: Realization of Multiplier using Delay Efficient Cyclic Redundant Adder** Dheepika K, Jevasankari K S, Vippin Chandhar and Binsu Kailath.
PID 112(S): Fast Architecture of Modular Inversion using Itoh-Tsujii Algorithm Pravin Zode, Abdus Samad and Raghavendra Deshmukh.	
Analog/Mixed Signal	
PID 37: Low Voltage, Low Power Transconductor for Low Frequency Gm -C Filters Hanumantha Rao G. and Rekha S.	**PID 116: An improved highly efficient low input voltage charge pump circuit.** Naresh Kumar, Raja Hari Gudlavalleti and Subash Chandra Bose.
PID 169: Characterization and compensation circuitry for piezo-resistive pressure sensor to accommodate temperature induced variation Santosh Manabala, Anjli Bansal, Jitendra Mishra, Kanhu Charan Behera and Subash Chandra Bose.	**PID 98: A Calibration Technique for Current Steering DACs - Self Calibration with Capacitor storage.** Pallavi Darji and Chetan Parikh

PID 291: FEM based Device Simulator for High Voltage Devices Ashok Ray, Gaurav Kumar, Sushanta Bordoloi, Dheeraj Kumar Sinha, Pratima Agarwal and Gaurav Trivedi.	
VLSI Testing	
PID 18: Deterministic Shift Power Reduction in Test Compression Kanad Basu, Rishi Kumar, Santosh Kulkarni and Rohit Kapur.	**PID 20: Pseudo-BIST: A Novel Technique for SAR-ADC Testing** Yatharth Gupta, Dr. Sujay Deb, Vikrant Singh, V N Srinivasan, Manish Sharma and Sabyasachi Das.
PID 38: SFG-based Fault Simulation of Linear Analog Circuits using Fault Classification and Sensitivity Analysis Rahul Bhattacharya, S.H.M Ragamai and Subindu Kumar.	**PID 175: A Cost Effective Technique for Diagnosis of Scan Chain Faults** Satyadev Ahlawat, Darshit Vaghani, Jaynarayan Tudu and Ashok Suhag.
PID 185:Multi-mode Toggle Random Access Scan to Minimize Test Application Time Anshu Goel and Rohini Gulve.	
Devices and Technology – I	
PID 265: Vertical Nanowire FET Based Standard Cell Design Employing Verilog-A Compact Model for Higher Performance Satish Maheshwaram, Om Prakash, Mohit Sharma, Anand Bulusu and Sanjeev K Manhas	**PID 65: Low-Power Sequential Circuit Design using Work-function Engineered FinFETs** Ashish Soni, Abhijit Umap and Nihar R. Mohapatra.
PID 74(S): An Efficient VLSI Architecture for PRESENT Block Cipher and its FPGA Implementation Jai Gopal Pandey, Tarun Goel and Abhijit Karmakar.	**PID 164: Analysis of Electrolyte-Insulator-Semiconductor Tunnel Field-Effect Transistor as pH sensor** Ajay Singh, Rakhi Narang, Manoj Saxena and Mridula Gupta.
PID 236: Exploiting Characteristics of Steep Slope Tunnel Transistors towards Energy Efficient and Reliable Buffer Designs for IoT SoCs Aditya Japa, Harshita Vallabhaneni and Ramesh Vaddi.	

VDAT 2017 Program (Tentative)	
1st July 2017 (Day-2) (Management Block)	
Registration (MB Foyer)	
Time	**Event**
07:30 AM - 8:45 AM	Breakfast (Ravindra Bhawan Lounge)
09.00 AM - 9:45 AM	**Invited Speaker - 3 (Prof Maryam Shojaei, IIT-Bombay)**
9.45 AM - 10.30 AM	**Invited Speaker - 4 (Dr Sudarshan Kumar, HSMC)**
10:30 AM - 10.45 AM	Tea Break (Management Block Central Lawn)
10.45 AM - 12.45 PM	D2-I A, VLSI Architectures
	D2-I B, Emerging Technologies & Memory
12:45 PM to 01:45 PM	Lunch Break (Ravindra Bhawan Lounge)
01:45 PM to 03:45 PM	D2-II A, Devices and Technology-II
	D2-II B, System Design
3:45 PM to 4:15 PM	Poster Display and Tea Break
04:15 PM to 05:30 PM	Panel Discussion (VLSI Education)
05:30 PM to 08:30 PM	Haridwar Visit Tentative (Availability of at least 30 participants)
09.00 PM -10.00 PM	Banquet Dinner (Community Center)

VLSI Architectures	
PID 14: Energy-Efficient VLSI Architecture & Implementation of Bi-Modal Multi-Banked Register-File Organization Sumanth Gudaparthi and Rahul Shrestha.	**PID 115: Performance-Enhanced d^2-LBDR for 2D Mesh Network-on-Chip** Anugrah Jain, Vijay Laxmi, Meenakshi Tripathi, Manoj Singh Gaur and Rimpy Bishnoi.
PID 233: ACAM: Application Aware Adaptive Cache Management for Shared LLC Sujit Kr Mahto and Newton Singh.	**PID 85(S): Adaptive Packet Throttling Technique for Congestion Management in Mesh NoCs** N. S. Aswathy, R. S. Reshma Raj, Abhijit Das, John Jose and V. R. Josna.
PID 131(S): Defeating Hatch - Building Malicious IP Cores Anshu Bhardwaj and Subir Kumar Roy.	
Emerging Technologies & Memory	
PID 207: Modeling and Analysis of Transient Heat for 3D IC Subhajit Chatterjee, Surajit Roy, Chandan Giri and Hafizur Rahaman.	**PID 235: Low Write Energy STT-MRAM Cell using 2T- Hybrid Tunnel FETs exploiting the Steep Slope and Ambipolar Characteristics** Sudha Vani Yamani, Usha Rani Nelakuditi and Ramesh Vaddi.
PID 194: Memory Efficient Fractal-SPIHT based Hybrid Image Encoder Mamata Panigrahy, Indrajit Chakrabarti, Anindya Sundar Dhar, Nirmal Behera and B Vandana.	**PID 274: Metal-Oxide Nanostructures designed by Glancing Angle Deposition Technique and its applications on Sensors and Optoelectronic Devices** Divya Singh.
PID 241(S): Enhancing Retention Voltage for SRAM Suprateek Shukla, Ankit Rehani and Sujay Deb.	

Devices and Technology – II	
PID 160: Delay and Frequency Investigations in Coupled MLGNR Interconnects Manish Joshi, Koduri Teja, Ashish Singh and Rohit Dhiman.	**PID 165: LISOCHIN: An NBTI Degradation Monitoring Sensor for Reliable CMOS Circuits** Ambika Prasad Shah, Nandakishor Yadav and Santosh Kumar Vishvakarma.
PID 168: Performance Analysis of OLED with Hole Block Layer and Impact of Multiple Hole Block Layer Shubham Negi, Poornima Mittal and Brijesh Kumar.	**PID 192: A Cost Effective Technique for Diagnosis of Scan Chain Faults** Satyadev Ahlawat, Darshit Vaghani, Jaynarayan Tudu and Ashok Suhag.
PID 174: Improved Gate Modulation in Tunnel Field Effect Transistors with non-rectangular tapered Y-Gate geometry Rakhi Narang, Mridula Gupta and Manoj Saxena.	**PID 252(S): A 10T Subthreshold SRAM Cell with Minimal Bitline Switching for Ultra-low Power Applications** Swaati and Bishnu Prasad Das.
System Design	
PID 133: A High Speed KECCAK Coprocessor for Partitioned NSP Architecture on FPGA Platform Rourab Paul and Sandeep Kumar Shukla.	**PID 190: New Energy Efficient Reconfigurable FIR Filter Architecture And Its FPGA Implementation** Naushad Ali and Bharat Garg.
PID 240: FPGA-based Smart Camera System for Real-time Automated Video Surveillance Sanjay Singh, Sumeet Saurav, Ravi Saini, Atanendu S. Mandal and Santanu Chaudhury.	**PID 139: Effectiveness of High Permittivity Spacer for Underlap regions of Wavy-Junctionless FinFET at 22 nm node and Scaling Short Channel Effects** B Vandana, J K Das, S K Mohapatra and B K Kaushik.
PID 278(S): A Custom Designed RISC-V ISA Compatible Processor for SoC Kavya Sharat, Sumeet Bandishte, Kuruvilla Varghese and Amrutur Bharadwaj.	**PID 166: Design and Implementation of Ternary Content Addressable Memory (TCAM) based Hierarchical Motion Estimation for Video Processing** Puja Ghosh and P. Rangababu.

VDAT 2017 Program (Tentative)	
2nd July 2017 (Day-3) (Management Block)	
Registration (MB Foyer)	
Time	**Event**
07:30 AM - 8:30 AM	Breakfast (Ravindra Bhawan Lounge)
09.00 AM - 11:00 AM	D3-I A, Low Power Design & test
	D3-I B, RF Circuits
11.30 AM - 11.15 AM	Tea Break (Management Block Central Lawn)
11:15 AM - 12:00 Noon	**Invited Speaker – 5 (Mr. Subhasish, Cadence)**
12.00 Noon - 12.45 PM	**Invited Speaker – 6 (Prof. Masahiro Fujita, Tokyo University)**
01:30 PM - 2:15 PM	Lunch Break
02:15 PM to 04:15 PM	D3-II A, Architecture and CAD
	D3-II B, Design Verification
04:15 PM to 04:45 PM	Valedictory Ceremony (MAC Auditorium)

Low Power Design & Test	
PID 22: An Efficient Timing and Clock Tree Aware Placement Flow with Multibit Flip-Flops for Power Reduction Jasmine Kaur Gulati, Bhanu Prakash and Sumit Darak.	**PID 266: On Generation of Delay Test with Capture Power Safety** Rohini Gulve and Nihar Hage.
PID 222: Primitive Instantiation based Fault Localization Circuitry for High Performance FPGA Designs Ayan Palchaudhuri and Anindya Sundar Dhar.	
RF Circuits	
PID 47: A 10MHz, 42ppm/ , 69 µW PVT Compensated Latch Based Oscillator for PCM Vivek Tyagi, Mohammad S.Hashmi, Ganesh Raj and Vikas Rana.	**PID 52: A 1.8V Gain Enhanced Fully Differential Doubly-Recycled Cascode OTA with 100dB gain 200MHz UGB in CMOS** Antaryami Panigrahi and Abhipsa Parhi.
PID 88: A Low Power, Frequency-to-Digital Converter CMOS Temperature Sensor in 65 nm Process Mudasir Bashir, Patri Sreehari and K S R Krishna Prasad.	**PID 105: Design & Development of HighSpeed LVDS Receiver with cold-spare feature in SCL's 0.18um CMOS Process** Munish Malik, Ajay Kumar and H.S Jatana.
Architecture and CAD	
PID 66: Fast FPGA Placement Using Analytical Optimization Sameer Pawanekar and Dr. Gaurav Trivedi.	**PID 67: Analytical Partitioning : Improvement over FM** Sameer Pawanekar and Dr. Gaurav Trivedi.
PID 89: A Dependability Preserving Fluid-level Synthesis for Reconfigurable Droplet-based Microfluidic Biochips Arpan Chakraborty, Piyali Datta, Debasis Dhal and Rajat Pal.	**PID 159: Splitting and Transport of a Droplet with no external actuation force for Lab on Chip Devices** T Pravinraj and Rajendra Patrikar.

PID 192: A 36nW Power Managment Unit for Solar Energy Harvesters using 0.18um CMOS Purvi Patel, Biswajit Mishra and Dipankar Nagchoudhury.	
Design Verification	
PID 30: A Formal Perspective on Effective Post-silicon Debug and Trace Signal Selection Binod Kumar, Kanad Basu, Ankit Jindal, Brajesh Pandey and Masahiro Fujita.	**PID 41: Translation Validation of Loop Invariant Code Optimizations Involving False Computations** Ramanuj Chouksey, Chandan Karfa and Purandar Bhaduri.
PID 197: A Framework for Automated Feature Based Mixed-Signal Equivalence Checking Antara Ain, Sayandeep Sanyal and Pallab Dasgupta.	**PID 239: xMAS Based Accurate Modeling and Progress Verification of NoCs** Surajit Das, Santosh Biswas and Chandan Karfa.